Research · Report NR-07 · 23 September 2026

A logic gate made of light: the N1 cell in cascade

With the best published silicon components, an opto-electronic gate has gain, but loses the signal after a few cells and uses about 16,000 times the energy of a transistor.

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Refuted

simulation, not measurement · 12 seeds · 13,000 bits per chain · every parameter sourced

2.13	0.01	~16,000×	2520
gain of the cell, above the threshold of 2 (the only criterion passed)	signal quality at cell 10, against 7 required	energy per operation compared with a CMOS transistor	configurations tried in the declared calibration

SUMMARY

A digital brain might one day run on a substrate other than electronic silicon. The first question we asked was the simplest: can a logic gate useful for a photonic processor be built with silicon components that have already been published? A useful gate must meet Miller's requirements (2010): gain, level restoration, cascadability, temperature tolerance and an energy cost comparable with electronics. The N1 cell is an inverter: a germanium photodiode receives the input light and charges an electrical node connected to a microdisk modulator (Timurdogan and colleagues, MIT, 2014), which lets the light of a laser through or blocks it. With every parameter taken from a paper, the cell has gain (2.13), but the signal dies out after a few cells, the levels stay stable only within a range of half a degree and no speed passes the bench. The energy is 10.6 pJ per operation, about 16,000 times a CMOS transistor. **The prediction written in advance is refuted.**

1 The question

The Nadirion project asks on what physical matter a digital brain could run. Before simulating brain circuits on photonic devices (NR-08) we wanted to know whether the silicon photonics available today offers at least one logic gate that can be cascaded. It is a preliminary, exploratory question at zero cost: no chip was fabricated.

2 The N1 cell

The input light hits a germanium photodiode (DeRose and colleagues, Sandia, 2011) that charges a small electrical node. The node is connected to the junction of a microdisk modulator: the voltage shifts the disk's resonance, which lets through or blocks the light of a laser on a waveguide. So light controls light, and the output is the inverse of the input. The gain is paid for by the laser, just as the power supply pays for that of a transistor.

3 Method

1. **Criteria written in advance**, approved by the author on 23 September: gain ≥ 2 with two outputs connected (C1); noise margins ≥ 20% of the swing (C2); 10 cells in cascade with signal quality Q ≥ 7, stable levels and restoration of a degraded input (C3); tolerance of ±1 K (C4); energy compared with CMOS (C5, descriptive); at least 1 Gb/s (C6).
2. **Sourced parameters.** Every number from a paper we read, with a figure or table; no value better than the best published device. Disk, junction and losses from the MIT device alone, so as not to combine different devices; thermal model from the Trento group (Borghi, Pavesi and colleagues, 2021); heaters and fabrication variability from Parsons and colleagues (2025); CMOS reference from the IRDS 2022 roadmap (0.65 fJ).
3. **Instrument check.** The simulator integrates the equations in time and must reproduce the device data, conserve energy and give the theoretical thermal noise: passed.
4. **Calibration** on a declared grid of 2520 combinations (polarity, voltages, resistance, detuning from the laser, power), with a speed constraint written in advance.
5. **Bench** on 12 seeds, validation 0–5 and confirmation 6–11, 13,000 bits per chain.

4 Results

criterion	outcome	value
C1 gain	passed	2.13, at most two outputs
C2 margins	failed	low margin 0.003 against 0.20
C3 cascade at 1 Gb/s	failed	Q 14.7 at cell 2, 7.5 at cell 3, 0.01 at cell 10
C4 temperature	failed	levels stable only between −0.4 and +0.1 K
C6 speed	failed	no frequency passes
C5 energy	level B	10.6 pJ per operation, about 16,000 times CMOS

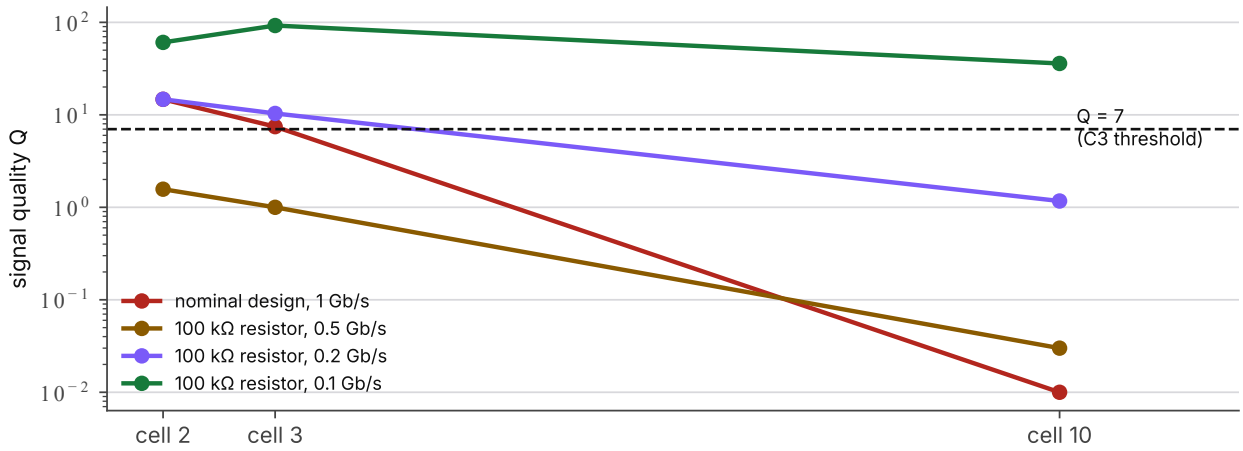


Figure 1. Signal quality Q along a chain of 10 cells, for the nominal design at 1 Gb/s and for a design with a 100 kΩ resistor at lower speeds (seed 0; the other 11 seeds give almost identical values). The nominal design loses the signal after the third cell. With 100 kΩ at 0.1 Gb/s the signal reaches cell 10, but the levels do not restore a degraded input. Data from the transcript of the bench of 23 September 2026.

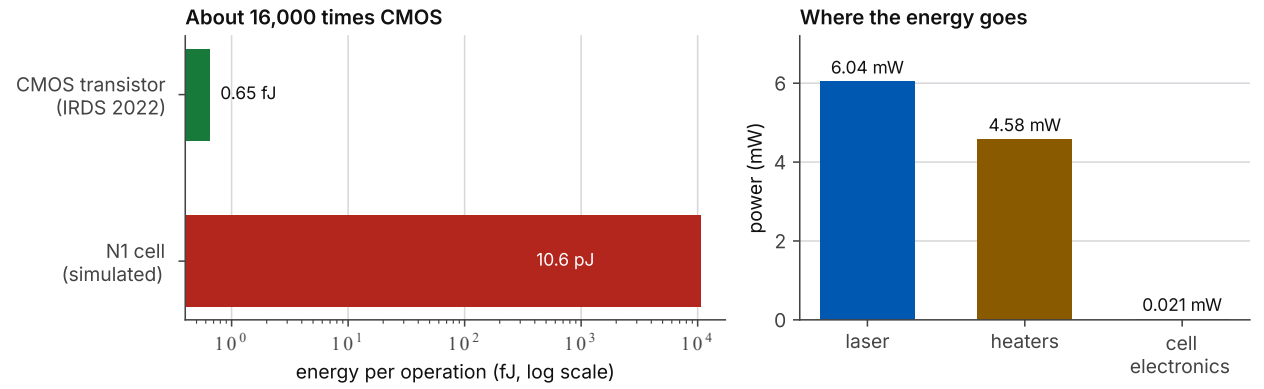


Figure 2. Left, the energy per operation of the simulated N1 cell against a CMOS transistor (log scale). Right, where the power goes: the laser, with an efficiency of about 10% and its losses, and the heaters that compensate for fabrication variability. The device itself uses a negligible share.

5 Why it does not work

Three constraints contradict each other. **Gain** requires large resistances, **speed** requires small ones, and raising the laser power **heats** the disk: 8.4 K per milliwatt, against about 3 K needed to shift the resonance by one linewidth. The heat creates hysteresis or opposes the signal. The energy is dominated by the laser and the heaters, not by the device. With the pessimistic parameters the gate does not even have two stable levels.

6 Corrections along the way

All recorded in the record, before using the bench seeds:

- linewidth from 0.17 nm (read by eye) to 0.31 nm (graph) to **0.25 nm** (text of the paper, 30 GHz);
- photodiode responsivity from 0.8 A/W (abstract) to **0.26 A/W** at the device's wavelength;
- two inconsistencies in the source itself documented and not resolved;
- a fast variant of the simulation discarded because it did not pass the recorded check (1.09% against 1%);
- a bench error found by the smoke test, corrected before the run.

7 What it shows and what it does not

It shows that with this device and these components a cascaded opto-electronic gate does not meet the requirements of useful logic, and that the energy cost is dominated by laser and heaters.

It does not show that no opto-electronic gate can work: the refutation holds for the N1 cell with this device, without optimising the device. Heater, thermal behaviour and carriers come from different devices, and their combination has not been demonstrated.

According to the rule written in advance, the "photonic logic" line stopped here, and we moved on to the next question: a brain circuit on laser neurons (NR-08).

> **Limitations.** Simulation, not measurement. The node cannot leave the voltage range measured in the paper. Values read from graphs have a declared uncertainty. No chip was fabricated.

References

- Miller, D. A. B. (2010). Are optical transistors the logical next step? *Nat. Photon.* 4, 3.
- Timurdogan, E. and colleagues (2014). An ultralow power athermal silicon modulator. *Nat. Commun.* 5, 4008.
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- IRDS 2022, More Moore.
- Internal documents: whitepaper WP-P1; record `photonics/registry/p1_cella_n1.yaml`; logs `p1_c0_20260923_1739`, `p1_taratura_20260923_1959`, `p1_banco_20260923_2118`.

How to cite

Chiarolanza, G. (2026). A logic gate made of light: the N1 cell in cascade. Nadirion, research report NR-07, 23 September 2026. https://nadirion.eu/en/research/photonic-logic-gate/

Nadirion technical report, not peer-reviewed. The criteria of every test were written before running it; negative results are reported like positive ones. The tests measure functional roles.